What Is Claimed Is:

1. A synchronous dynamic memory operating in synchronized with an external clock, comprising:

a clock input buffer receiving said external clock and outputting an internal clock;

a command input buffer receiving commands in synchronization with said internal clock;

an address input buffer receiving addresses in synchronization with said internal clock; and

a data input buffer receiving data in synchronization with said internal clock;

wherein said clock input buffer supplies said internal clock to said command, address, and data input buffers in normal operation mode, and wherein said clock input buffer supplies said internal clock to said command input buffer and stops supply of said internal clock to said address input buffer or data input buffer in data hold mode.

2. The synchronous dynamic memory according to claim 1, further comprising:

a first clock supply line that supplies said internal clock to said command input buffer; and

a second clock supply line that supplies said internal clock to said address input buffer or said data input buffer;

wherein said clock input buffer drives said first

and second clock supply lines in normal operation mode, and said clock input buffer drives said first clock supply line and stops driving said second clock supply line in said data hold mode.

3. The synchronous dynamic memory according to claim 2, wherein said first clock supply line is shorter than said second clock supply line.

4. The synchronous dynamic memory according to claim 1, wherein said clock input buffer receives a clock enable signal that distinguishes between normal operation mode and power down mode, and said data hold mode includes this power down mode.

5. A synchronous dynamic memory operating in synchronized with an external clock, comprising:

a clock input buffer receiving the external clock and outputting an internal clock;

a command input buffer receiving commands in synchronization with said internal clock;

an address input buffer receiving addresses in synchronization with said internal clock; and

a data input buffer receiving data in synchronization with said internal clock;

wherein said clock input buffer supplies the internal clock to said command, address, and data input

buffers in normal operation mode, supplies the internal clock to said command input buffer and stops supplying a clock to said address input buffer or said data input buffer in data hold mode without being accessed for read/write, and stops supplying the internal clock internally in power down mode.

6. The synchronous dynamic memory according to claim 5, comprising:

a first clock supply line that supplies said internal clock to said command input buffer; and

a second clock supply line that supplies said internal clock to said address input buffer or said data input buffer;

wherein said clock input buffer drives said first and second clock supply lines in normal operation mode, drives said first clock supply line and stops driving said second clock supply line in said data hold mode, and stops driving said first and second clock supply lines in power down mode.

7. The synchronous dynamic memory according to claim 6, wherein said first clock supply line is shorter than said second clock supply line.

8. The synchronous dynamic memory according to claim 5, wherein said clock input buffer inputs a first signal

that distinguishes between normal operation mode and power down mode and a second signal that prompts said data hold mode.

9. An LSI, wherein the synchronous dynamic memory described in any one of claims 1 through 8 is embedded on one chip with a processing circuit macro that implements a prescribed processing.

10. The LSI according to claim 9, further comprising a memory controller that controls said synchronous dynamic memory.

11. A synchronous dynamic memory operating in synchronized with an external clock, comprising:

a clock input buffer receiving the external clock and outputting an internal clock;

a command input buffer receiving commands in synchronization with said internal clock;

an address input buffer receiving addresses in synchronization with said internal clock; and

a data input buffer receiving data in synchronization with said internal clock;

wherein a signal that distinguishes between a first operation mode and a second operation mode is supplied to said clock input buffer, and

wherein said clock input buffer supplies said

internal clock to each of said command, address, and data input buffers in said first operation mode, and supplies said internal clock to said command input buffer and stops supplying the internal clock to said address input buffer or said data input buffer in said second operation mode.

12. A semiconductor integrated circuit that fetches input signals in synchronization with an internal clock signal generated by a clock buffer, comprising:

a clock buffer controller that activates said clock buffer only when there is a change in said input signals.

13. The semiconductor integrated circuit according to claim 12, further comprising an input buffer that generates an internal signal from said input signal in synchronization with said internal clock signal.

14. The semiconductor integrated circuit according to claim 13, wherein said clock buffer controller compares said input signal with said internal signal output from said input buffer and activates said clock buffer when said input signal differs from said internal signal.

15. A semiconductor integrated circuit comprising:

a plurality of input buffers that fetches input signals in synchronization with internal clock signal generated by a clock buffer; and

a clock buffer controller that activates said clock buffer when there is a change in said input signal input into at least one of said input buffers.

16. The semiconductor integrated circuit according to claim 15, wherein said clock buffer controller are provided to correspond with each of said input buffers, and each said clock buffer controller includes a plurality of signal change monitoring circuit that activate said clock buffer when there is a change in said input signal input into said input buffer.

17. The semiconductor integrated circuit according to claim 16, wherein said signal change monitoring circuit includes a comparative circuit that compares said input signal with signal output from said input buffer, and

wherein said clock buffer controller further includes a logic circuit that logically synthesizes signals output from a plurality of said comparative circuits, generates an activation signal that activates said clock buffer, and supplies the activation to said clock buffer.

18. The semiconductor integrated circuit according to claim 17, wherein said logic circuit logically synthesizes signals output from a plurality of said comparative circuits into which the same type of signals are input.

19. A signal fetching method for fetching input signals in synchronization with an internal clock signal generated by a clock buffer in a semiconductor integrated circuit, comprising a step for activating said clock buffer only when there is a change in said input signal.

20. A signal fetching method for fetching input signals in synchronization with an internal clock signal generated by a clock buffer at a plurality of input buffers in a semiconductor integrated circuit, comprising a step for activating said clock buffer when there is a change in at least one of said input signals supplied to said input buffer.